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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,234	SHAH, EMANUEL E.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for benefit under 35 U.S.C. 119(e).

Claim Objections

2. Claims 1-20 are objected to because of the following informalities:

The claims are replete with grammatical errors. For example:

In claim 1, line 2, the word "instruction" should be preceded with the article "an".

In, claim 1, line 9, the article "a" does not agree with the plural "branch or jump instructions" and should be deleted.

In claim 1, line 11, the article "an" should precede the word "address".

In line 2 of claims 4-7 and 9-12, the article "a" prior to the word "logic" should be deleted.

In claim 4, line 2, the word "allow" should be replaced with the word "allows".

In claim 4, line 3, the phrase "of a" should be deleted.

In claim 5, line 2, the article "a" should precede the term "non pipelined".

In claim 5, line 4, the word "allows" should be replaced with the word "allows".

In claim 9, line 2, the article "the" should precede the word "same".

In claim 14, line 2, the article "an" should precede the word "external".

The above list is not exhaustive. It is suggested that Applicant proofread the claims and make changes where necessary. Appropriate correction is required.

Claim 17 contains a misplaced period on line 53. The period should be deleted and replaced with a semicolon.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 4-8 and 11-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 4 recites logic in the CPU that allows recently used data to be stored in the transition buffer. Although support is found in the specification for the storing of recently used data in the transition buffer (Page 22, lines 10-19, page 25, lines 11-20), a description of logic in the CPU that allows the aforementioned storing is not found in the specification.

Claims 5 and 6 contain similar deficiencies as claim 4. Claims 5 and 6 recite that the CPU includes a memory area that allows recently used data to be stored in the transition buffer. A description of a memory area in the CPU that allows the aforementioned storing is not found in the specification.

Claim 7 recites logic in the CPU for implementing pipelined storage in main memory. Although support is found in the specification for pipelined storage in main memory (Page 24, lines 10-11), a description of logic in the CPU for implementing the pipelined memory is not found in the specification.

Claims 11 and 12 recite a storage area included in the CPU for storing data available to the CPU and related to the main execution memory. While the specification is well enabling for a storage area, the specification does not describe this storage area as being included in the CPU.

For the purposes of examination, the limitations not supported by the specification as detailed above will be ignored.

All dependent claims are rejected under the same rationale as the claims they depend from.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The terms "low cost," "low power," "high speed," and "slower access time," in claims 1-20 are relative terms which render the claims indefinite. The terms are not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. See MPEP § 2171, 2173.05(b).

For the purposes of examination, these terms will be ignored.

Further, regarding claims 1-20, the word "means" is preceded by the word(s) "memory," "transition buffer," "address controller," and "direct access memory" in an attempt to use a "means" clause to recite a claim element as a means for performing a specified function. However, since no function is specified by the word(s) preceding "means," it is impossible to determine the equivalents of the element, as required by 35 U.S.C. 112, sixth paragraph. See *Ex parte Klumb*, 159 USPQ 694 (Bd. App. 1967).

For the purposes of examination, the term "means" will be ignored.

Claim 8 is not comprehensible. Accordingly, prior art has not been applied to this claim.

Claim 13 is not comprehensible. Accordingly, prior art has not been applied to this claim.

All dependent claims are rejected under the same rationale as the claims they depend from.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6, 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mekhiel (US 6,587,920) in view of Goodnow (US 5,918,246) and Sen (Subhabrata Sen et al, "Proxy Prefix Caching for Multimedia Streams," IEEE, Mar. 1999).

As in claim 1, Mekhiel discloses a system comprising:

a central processing unit (CPU) (Fig. 1, element 15; column 7, lines 57-62), where it is readily apparent that the CPU fetches and executes instructions from a computer program;

a main execution memory (Fig. 1, element 30; column 7, lines 57-62) comprising a plurality of banks (Column 6, lines 65-67; column 16, lines 11-15), where it is also apparent that the main memory stores the computer program;

a buffer comprising memory that stores starting locations of recently used data (Fig. 2; column 8, line 33 to column 9, line 8; Fig. 3, element labeled "BUFFER", column 9, lines 39-67), where it is again apparent that the data stored in the buffer comprises program and data segments;

an address controller for generating an address for accessing the remainder of the program and data segments from the main memory (Fig. 1, element 30; Fig. 3, element labeled "MEMORY CONTROLLER"; Figs. 4-5, elements 20, 230 and 240; column 10, lines 1-64);

a first address bus, a second data bus, and a third control bus for communicating address, data, and control information between the CPU, main memory, buffer and address controller (Fig. 1, elements 16 and 18-19; column 7, line 57 to column 8, line 6);

wherein the CPU couples with the main memory for fetching data (Fig. 6, steps 300, 310, 330, 340 and 350; column 11, lines 31-51);

the CPU couples with the buffer for fetching starting memory locations of data (Fig. 6, steps 300, 390, 400 and 410; column 12, lines 4-17);

the CPU further couples with the address controller and main memory while the starting memory locations are accessed, and allows enough time for the main memory to access and output data for the CPU to fetch (Fig. 6, steps 430 and 440; column 12, lines 4-12 and 18-29);

where it is readily apparent in the above steps that the data from both the buffer and main memory comprises instructions that are executed by the CPU in the sequence that they are fetched, that at the start of the program the data would not yet be located in the buffer, and that the instructions are executed until a new fetch is required.

Mekhiel does not teach that the starting memory locations stored in the buffer are characterized by branch or jump instructions such that when a jump or branch instruction is encountered the CPU retrieves the starting memory locations of program branch instructions from the buffer as required by claim 1.

Mekhiel also does not teach that the remaining instructions are fetched from the main memory until completion of the program or a new program branch as required by claim 1.

Goodnow teaches a system where starting memory locations of program branch instructions are stored in a buffer (i.e. cache) such that when a jump or branch instruction is encountered by the CPU, the instructions and data are retrieved from the buffer (Abstract; Figs. 1-5; column 8, lines 35-64). Goodnow teaches that this avoids CPU stalls caused by program branching (Column 8, lines 55-58).

Sen teaches a system for delivering large multimedia objects where an initial portion of the data is delivered from a cache for low latency access, while simultaneously requesting the remainder of the data from main storage, and finally delivering the remaining portion obtained

from main storage (Page 1310, Introduction, paragraph 1, lines 13-16, paragraph 3, lines 1-11). Sen teaches that this arrangement allows conservation of cache storage space (Page 1310, Introduction, paragraph 1, lines 5-13).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to store starting memory locations of program branch instructions in a buffer such that when a jump or branch instruction is encountered by the CPU, the starting memory locations of program branch instructions are retrieved from the buffer as taught by Goodnow, in the system of Mekhiel, where the buffer in Goodnow corresponds to the buffer in the system of Mekhiel, in order to avoid CPU stalls caused by program branching as taught by Goodnow.

Further regarding claim 1, the teachings of Sen would suggest to one of ordinary skill in the art that a stream of program data retrieved from a main memory could be treated in a similar way as the video data stream retrieved from server storage as in Sen, due to the similar nature of the problems, namely to deliver a large stream of data with low latency while conserving buffer space. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to fetch the remaining instructions from main memory as suggested by the teachings of Sen, in the system made obvious by the combination of Mekhiel and Goodnow, in order to conserve space in the cache as taught by Sen.

As in claim 2, Mekhiel discloses that the main memory is comprised of dynamic random access memory (DRAM) (Column 14, lines 30-38). Although Mekhiel does not explicitly state that the buffer is comprised of static random access memory (SRAM), Mekhiel does teach that similar buffers are comprised of SRAM due to their speed advantage over DRAM (Column 2, lines 14-25), and therefore it would have been obvious to one skilled in the art to make the buffer using SRAM.

Regarding claims 4-6, relying on the rationale for the rejection of claim 1, it is noted that the recently used data stored in the buffer of Mekhiel, as well as the data stored in the buffer of Goodnow comprises both instructions and data, and that Mekhiel stores recently used instructions and data in the buffer. Furthermore, Mekhiel also discloses a separate memory area for storing recently used data in conjunction with the buffer (Fig. 3, elements labeled "L1 CACHE" and "L2 CACHE").

As in claims 11-12, relying on the rationale for the rejection of claim 1, the buffer of Mekhiel by definition is a storage area that stores data available to the CPU and related to the main memory, however the combination of Mekhiel and Goodnow as applied to claim 1 above does not teach that data can be selectively loaded and removed from the storage area based on the execution requirement of the program and conditions determined at compile time as required by claim 12.

Goodnow further teaches that the buffer is dynamically loaded during program execution (i.e. data is stored and removed) based on the program execution and a mapping determined at compile time (Column 3, lines 47-49; column 7, lines 7-42). Goodnow teaches that this enables maximum processing efficiency by approaching a 100% hit rate (Column 7, lines 39-42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to selectively load and remove data from the buffer based on the execution requirement of the program and conditions determined at compile time as taught by Goodnow, in the system made obvious by the combination of Mekhiel and Goodnow as applied to claim 1 above, in order to enable maximum processing efficiency by approaching a 100% hit rate as taught by Goodnow.

Claim 15 is rejected using the same rationale as for the rejection of claim 1, where it is noted that Goodnow clearly contemplates an interrupt as causing a branch or jump in a program execution flow (Column 2, line 44 to column 3, line 18).

Regarding claim 17, it is noted that claim 17 differs from claim 1 in two aspects. First, claim 17 includes limitations directed toward writing data that were not present in claim 1. Secondly, the combined instruction and data path of claim 1 is split into independent instruction and data paths according to the Harvard Architecture.

As to the first aspect of claim 17, Mekhiel teaches that the CPU writes starting locations of data to the buffer while allowing time for accessing the main memory, and then the CPU

writes the remaining data to the main memory (Fig. 6, steps 300, 390, 460, 480 and 490; column 12, lines 36-59).

As to the second aspect of claim 17, see Examiner's Official Notice below.

Examiner takes Official Notice of the following well-known teachings in the art:

Regarding claim 3, interleaving access among parallel groups of memory cells is well-known in the art as a way to hide latency and provide higher sustained bandwidth in a memory subsystem, and therefore it would have been obvious one of ordinary skill in the art to provide instructions to the CPU from one group of memory cells while another group is accessing subsequent instructions, in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Regarding claim 5, a non-pipelined architecture is well known in the art as a low-complexity design, and for this reason it would have been obvious to one of ordinary skill in the art to utilize such an architecture for the CPU, in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Regarding claim 6, a pipelined architecture comprising an instruction queue is well-known in the art as providing higher performance than a non-pipelined architecture, and for this reason it would have been obvious to one of ordinary skill in the art to utilize such an

architecture for the CPU, in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Regarding claim 9, logic for preventing simultaneous writing of the same location by more than one device is well-known in the art for avoiding potentially harmful contention in a system and to avoid writing erroneous data, therefore it would have been obvious to one of ordinary skill in the art to provide this logic in the CPU, in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Regarding claim 10, pre-decoding of instructions in a CPU is well known in the art in order to enable better scheduling and prediction of program execution, and for this reason it would have been obvious to one of ordinary skill in the art to provide this advanced decoding of instructions in the CPU, in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Regarding claim 14, it is well known in the art to transfer program and data segments from peripheral devices including hard drives to system memory using direct memory access (DMA), in order to allow the CPU to continue executing instructions in parallel with the transfer of the data, and therefore it would have been obvious to one of ordinary skill in the art to use DMA to transfer data and instructions into the buffer and main memory in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Regarding claim 16, it is well known in the art to manage power consumption in a computer system by turning off unused components of the system, and to do so would have been obvious in the system made obvious by the combination of Mekhiel, Goodnow and Sen.

Further regarding claim 17, the Harvard Architecture is a well known architecture in the art by which the instruction and data paths are separated to include separate memories for instructions and data from the main memory up through the memory hierarchy including buffers and caches. One advantage of the Harvard Architecture is that it allows instructions and data to be accessed simultaneously.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to split the instruction and data paths according to a Harvard Architecture resulting in separate instruction and data main memories and buffers, in the system made obvious by the combination of Mekhiel, Goodnow and Sen, in order to access instructions and data simultaneously.

Claim 19 is rejected using the same rationale as for the rejection of claim 1, and further noting that it is well known in the art to configure a plurality of CPU's with a shared memory system in order to improve processing performance while allowing sharing of data among processors.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to use a plurality of CPU's, in the system made obvious by the

combination of Mekhiel, Goodnow and Sen, in order to improve processing performance while sharing data among processors.

Claims 18 and 20 are rejected using the same rationale as for the rejection of claim 9.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mekhiel (US 6,587,920) in view of Goodnow (US 5,918,246) and Sen (Subhabrata Sen et al, "Proxy Prefix Caching for Multimedia Streams," IEEE, Mar. 1999) as applied to claim 1 above, and further in view of Young (Cliff Young et al, "Near-optimal Intraprocedural Branch Alignment," ACM, 1997) and Examiner's Official Notice.

Mekhiel, Goodnow and Sen are relied upon for the teachings relative to claim 1 as above.

The rationale derived from Examiner's Official Notice used in the rejection of claim 3 above is incorporated herein for the teaching of an interleaved main memory where one group of memory cells provides instructions while another group is accessed, where it is further noted that such an interleaved memory constitutes a pipelined memory storage.

The combination of Mekhiel, Goodnow and Sen does not teach that sequential starting locations of multiple branch instructions are stored in required order as determined at compile time as required by claim 7.

Young teaches a compile-time code reordering of program blocks where basic blocks characterized by branch instructions are aligned according to an expected order of execution such that the most likely follower of an instruction will be stored in sequence, thereby avoiding pipeline penalties (Page 183, Introduction, paragraphs 1-4). Although Young treats cache memories and execution pipelines, it is readily apparent from Young that the same teachings would apply to a pipelined main memory. Young teaches using a compiler to achieve high spatial locality in a code sequence with branches by storing the code in the required order of execution, where the result is avoidance of interrupting a pipeline fed by fetching the code sequence.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to store sequential starting locations of multiple branch instructions in required order as determined at compile-time, as taught by Young, in the system made obvious by the combination of Mekhiel, Goodnow and Sen, in order to avoid interruption of the pipeline as taught by Young.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMR

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